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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,174	01/26/2004	Toru Tanzawa	248110US2S	6702

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,174	TANZAWA ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 10-26-05 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Objections

Claim 5 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. As understood by the examiner, claim 1 reads on figure 13 of the present application. The resistor elements in claim 5 that depends upon claim 1 read on figure 4.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1, 2, 4-8 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "the output stage including **a common gate connected** to the control input" is indefinite because it is misdescriptive. Figure 4 of the present application shows that the output stage (121-124) is connected to the output of the output of the control circuit (116), not the control input of the control circuit as recited. It is also not clear what " a common gate" is meant by. The same rationale is applied to claim 9 for " the common gate" on lines 11 and 14 and the "common gate" in claims 16 and 21.

Claim 7 is indefinite because it is not clear what are the first and second currents. The Applicant is requested to show in what drawing claim 7 reads on and to show the first and second currents in the drawing.

Claim 15 is indefinite because it is misdescriptive. According to figure 4, the first and second currents are input currents to comparator (116). The capacitor is connected to the output of the comparator thus, there is no charging or discharging from the capacitor that is connected between the output of the comparator and ground.

Claims 2, 4-6 and 8 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7-10, 16-19 and 21-25 are ejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert (USP. 6,204,719) in view of Takai et al. (USP. 6,163,190).

Regarding claims 1, 2 and 21, figure 4 of Gilbert shows a signal level detector comprising: a first voltage /current conversion circuit (13), a second voltage /current conversion circuit (15), a control circuit (18A). The output current of the first and second voltage /current conversion circuit depend on the square of the input voltages. Figure 4 of Gilbert does not show that the signal level detector circuit includes an output stage comprising common gated connected transistors. However, It is old and well known in the art that an output stage or a buffer is used to buffer an output of a circuit or is used for signal modifying purpose. Figure 2 of Takai shows a buffer (20) used as an output stage coupled to the output of comparator (10) for modifying the output signal of the comparator. Therefore, it would have been obvious for one of ordinary skill in the art to implement the output circuit taught by Takai to the output of comparator (18A) of Gilbert for modifying the output signal of the signal level detector. The inputs to the circuit of Gilbert comprise differential signals.

Regarding claims 7 and 8, figure 6 of Gilbert shows that at node E1 current (It) flows out of the first voltage /current conversion circuit and current (It) flows into the second voltage /current conversion circuit. The direction of the current flows could be reversed if the electron flow is considered.

Regarding claims 9 and 10, figures 2 and 4 of Gilbert shows a signal level detector comprising: a first squaring circuit (13) receiving inputs (Vin+, Vin-), a second squaring circuit (15) receiving reference voltages (Vset+, Vset-), a control circuit (18A). The output current of the first and second voltage /current conversion circuit depend on the square of the input voltage. Figure 4 of Gilbert does not show that the control circuit comprises common gated connected transistors. However, It is old and well known in the art that an output stage or a buffer is used to buffer an output of a circuit or is used for signal modifying purpose. Figure 2 of Takai shows an output stage (20) coupled to the output of comparator (10) for modifying the output signal of the comparator. Therefore, it would have been obvious for one of ordinary skill in the art to implement the buffer (output circuit) taught by Takai to the output of circuit (18A) of Gilbert for modifying the output signal of the signal level detector Figure 2 shows that the first voltage applied to circuit (12) is detected based on the output (Vout).

Regarding claims 16, 17, 18 and 19, figure 2 of Gilbert shows an amplification factor control system comprising: an amplification circuit (26), a signal level detector including first voltage/current conversion circuit (12), a second voltage/current conversion circuit (14), a control circuit (18). Figure 2 of Gilbert does not show that the signal level detector circuit comprises an output stage comprising common gated connected transistors. However, It is old and well known in the art that an output stage or a buffer is used to buffer an output of a circuit or is used for signal modifying purpose. Figure 2 of Takai shows an output stage (20) coupled to the output of comparator (10) for modifying the output signal of the comparator. Therefore, it would have been obvious for one of ordinary skill in the art to implement the output stage taught by Takai to the output of the circuit of Gilbert for modifying the output signal of the comparator. Figure 2 shows that the output currents of circuit (12) and

(14) depends on the square of the output signal (28) and the square of the reference (Vset). The control signal (the output of circuit 18) increases/decreases with the output signal of the amplification circuit.

Regarding claims 22-25, the combination of Gilbert and Takai includes all the limitations of these claims wherein, figure 2 of Takai shows an output circuit comprising a PMOS (Tr2), an NMOS (Tr3) an two constant current sources (21) and (22).

Claims 4-6, 11-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert (USP. 6,204,719) in view of Kraz (US Pat. 6,563,319).

Regarding claims 4 and 5, figure 4 of Gilbert includes al the limitations of these claims except for the limitation that there are capacitors and resistors coupled between the outputs of the first and second voltage/current conversion circuits and the ground and a capacitor coupled to the output of circuit (18A). Figure 2 of Kraz shows a voltage conversion circuit having a capacitor (64) and a resistor (62) coupled between the output to the ground for charging and holding the output current of the voltage/current conversion circuit and for determining the decay of the output signal (col.5, lines 61-65; col. 6, lines 10-13). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to implement the capacitors and the resistors taught by Kraz into the circuit of Gilbert between the outputs of the voltage/current conversion circuits and the ground and between the output of the comparator (18A or 18 in figure 2) and the ground for charging and holding the output current of the voltage/current conversion circuits and for determining the decay of the output signal. Regarding claims 14 and 15, depending on the polarities of the comparator, the capacitor will be charged or discharged.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
12-28-05

TUAN T. LAM
PRIMARY EXAMINER